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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| EXAMINER |
|---|
| VIGUSHIN, JOHN B |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2827 | |

DATE MAILED: 04/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/039,131 | RABADAM ET AL. | |
| | Examiner | Art Unit | |
| | John B. Vigushin | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-12,14-19 and 22-28* is/are rejected.

7)☒ Claim(s) *4-6,13,20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### Rejections Based On Prior Art

1. The following references were relied upon for the rejections hereinbelow:

Salem (US 6,300,677 B1) Harada et al. (US 6,512,680 B2)

Hirashima et al. (US 6,335,566 B1) Lin et al. (US 5,239,198)

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 7, 9, 17-19 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salem.

A) As to Claims 1 and 17:

I. Salem discloses a package 80, in Fig. 4A, comprising: a substrate 84; an IC die 82 mounted on substrate 84 (col.4: 12-17); a charge pump including a passive component 86 mounted on and coupled to die 82 (col.4: 12-13; col.3: 66-col.4: 9).

II. Salem does not teach that the extension of component 86 from die 82 is less than or equal to 16 mils. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to limit the extension of component 86 from die 82 to less than or equal to 16 mils, depending on the spatial, mechanical and electrical requirements of an application, since it has been held that where the general

conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

B) As to Claims 2 and 18, Salem further discloses a BGA with multiple solder balls attached to substrate 84 (Fig. 4A; col.4: 12-23).

C) As to Claims 3 and 19, Salem further discloses component 86 is adhesively--i.e., solder--attached to die 82 (Fig. 4A; col.4: 12-13).

D) As to Claim 7, Salem further discloses component 86 is a capacitor (col.4: 10-11).

E) As to Claims 9 and 23, Salem further discloses package 80 uses Power Supply In Package Technology (i.e., the capacitors 86 of the charge pump are discrete components and mounted on the die 82 and substrate 84).

4. Claims 8 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Salem in view of Hirashima.

As to Claims 8 and 22:

I. Salem discloses all the limitations of base Claims 1 and 17, respectively, but does not disclose that package 80 is a molded array package.

II. Hirashima et al. discloses, in Fig. 23, an array package 2 injection molded with resin 17, said substrate 2 of package 1 having a well 40 carrying capacitors 16 (col.11: 12-20), the resin 17 protecting the capacitors and the active surface of the IC die.

III. Since both Salem and Hirashima et al. both teach a package with a well in the substrate that receives the capacitors, then protecting the capacitors and the active

surface of the IC die by molding the array package with a resin, as taught by Hirashima et al., would have been readily recognized in the pertinent art of Salem.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to mold the array package of Salem et al. with a resin in order to encapsulate and protect from dust and moisture the capacitors and the active surface of the IC die, as taught by Hirashima et al.

5. Claims 10-12, 14-16 and 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harada et al. in view of Lin et al.

A) As to Claims 10 and 24:

I. Harada et al. discloses, in Fig. 11: a package comprising: a substrate 140; an IC die 120 mounted on substrate 140 (col.8: 5-11); a BGA with multiple solder balls attached to a bottom surface of substrate 140 (col.8: 12-15); a charge pump including a passive component 112, 113 and electrically coupled to die 120 through substrate 140 (Fig. 11; col.2: 43-49).

II. Harada et al. does not teach: 1) a region of the bottom surface of substrate 140 free of the solder balls, 2) the passive component 112, 113 mounted on the region, and 3) the extension of the component 112, 113 from the bottom surface of the substrate is less than or equal to the extension of the solder balls from the bottom surface of the substrate.

III. Lin et al. discloses, in Fig. 7: a package 52 comprising: a substrate 12; an IC die 20 mounted on substrate 12; a BGA with multiple solder balls 32 attached to a bottom surface of substrate 12, the bottom surface including a region free of solder balls

32; a passive component 50 mounted on the region and electrically coupled to die 20 through traces 16, vias 18 and traces 14 of substrate 12 (col.6: 61-64; col.1: 46-52), wherein the extension of the passive component 50 is less than the extension of the balls 32 from the bottom surface of substrate 12 in order to be spaced from the motherboard 38. Lin et al. teaches that having components on two different levels (i.e., opposite sides) of the substrate enables the fabrication of a device having its dimensions or "footprint" as small as possible, which is demanded by the consumer electronics industry (col.8: 41-50; col.1: 26-35).

IV. Since both Harada et al. and Lin et al. are both practitioners in the same art of electronics packaging, the reduction of package dimensions for the purpose of making smaller consumer electronic devices, as taught by Lin et al., would have been readily recognized in the pertinent art of Harada et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the BGA on the bottom surface the substrate of Harada et al. by including a region free of solder balls, and mounting in said free region the passive components 112, 113 of the charge pump so that they extend from the substrate less than the extension of the solder balls of the BGA, in order that the passive components are safely spaced from the motherboard 122 as taught in Lin et al., and in order to form a compact package structure in Harada et al. that enables the fabrication of smaller electronic packages as desired in the electronics industry, as taught by Lin et al.

B) As to Claims 11 and 25, Harada et al. further discloses the component 112, 113 is surface mounted (Fig. 12) as does the modification in Lin et al. (component 50 in Fig. 7).

C) As to Claims 12 and 26, Harada et al. as modified by Lin et al. discloses that the adhesive attachment is solder paste 51 (Lin et al., col.6: 61-64).

D) As to Claim 14, modified Harada et al. further discloses that component 112 (and 113) is a capacitor (col.2: 43-45) (as does Lin et al. in col.6: 61-64).

E) As to Claims 15 and 27, modified Harada et al. further discloses that the package is a molded array package (col.8: 5-7) (as does Lin et al. in Fig. 7 and col.3: 67-col.4: 11).

F) As to Claims 16 and 28, modified Harada et al. further discloses the package uses Power Supply in Package technology (i.e., the capacitors 112, 113 of the charge pump are discrete components and mounted on the package substrate 122, as modified, above, by Fig. 7 of Lin et al.).

***Allowable Subject Matter***

1. Claims 4-6, 13, 20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

2. The following is a statement of reasons for the indication of allowable subject matter:

As to Claims 4 and 20, patentability resides in the limitation wherein *the adhesive attachment is user-dispensed epoxy*, in combination with the other limitations of the Claims 4 and 20, respectively.

As to Claims 5 and 21, patentability resides in the limitation wherein *the component and the die are electrically connected to the substrate using wire bonds*, in combination with the other limitations of Claims 5 and 21, respectively.

As to Claims 6 and 13, patentability resides in the limitation wherein *the component is an inductor*, in combination with the other limitations of Claims 6 and 13, respectively.

***Conclusion***

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wallace (US 6,040,622) discloses charge pumping capacitors C1-C10 for modifying a flash EEPROM (Fig. 4; col.3: 9-16), wherein said the charge pumping capacitors are mounted using Power Supply In Package technology; i.e., the charge pumping capacitors are mounted on the package substrate 24 and not integrated into the IC dice 50 and 52.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv
April 21, 2003